REMARKS

By this Amendment, claims 1, 4, 5 and 7 are amended merely to clarify the recited subject matter. Claims 1-8 are pending.

The Office Action objected to claims 4 and 7 for certain noted informalities; by this Amendment, those claims have been amended to correct the informalities. Therefore, the objection should be withdrawn.

The Office Action rejected claims 1-8 under 35 U.S.C. §102 as being unpatentable in view of Cloonan et al (US 5,724,352; hereafter "Cloonan"). Applicants traverse the rejection because Cloonan fails to disclose, teach or suggest scheduling means for data switching apparatus having a plurality of input ports and a plurality of output ports, the scheduling means including "a first pipeline stage for receiving a first set of requests and satisfying at least one of the first set of requests; [and] a priority mixer for determining a further set of requests, the further set including requests of said first set which were not satisfied and requests included in said plurality of requests which were not part of said first set and which are of any of said priority levels, independently of said priority levels," as recited in independent claim 1 and its dependent claims 2-8.

As indicated in the specification, the present invention relates to scheduling means for data switching apparatus for use in computer-controlled digital data switching systems. In particular, the invention, as recited in independent claim 1, provides scheduling means capable of insuring a combination of prioritization, fairness and efficiency. As explained herein, prioritization and fairness come from the scheduling means being capable of presenting requests of only one priority level to a first pipeline stage, where higher priority requests are presented more often than lower priority requests in proportion to the respective required bandwidth allocation for each of the priority levels.

As illustrated in Applicants' Figure 1, a first pipeline stage receives requests for connections RVi at a single priority level Pi. The first pipeline stage then attempts to satisfy as many of these requests as possible. Traffic of each priority level is presented to the first pipeline stage 10 at a frequency proportional to the required bandwidth allocation for that priority level. For example, higher priority level requests could be presented 60% of the time if a 60% bandwidth allocation for high priority traffic was required. The proportions assigned to each priority level do, of course, depend on the application and may be assigned by a system administrator and be independent of the operation of the pipeline stage.

However, typically two thirds of the requests provided to the first pipeline stage will be satisfied by the first pipeline stage. Given that the requests may be provided to the first

pipeline stage 10 in proportion to their respective priority levels, the proportion of satisfied requests reflects those priority levels. In other words, if 60% of the requests presented are of high priority and 40% are of low priority, 60% of the satisfied requests will be the high priority requests and 40% the low priority requests.

After the first pipeline stage, the requests are provided to a priority mixer 13. The priority mixer is also arranged to receive unsatisfied requests RVi from the first pipeline stage and in addition requests RV2i of any other priority levels. Indeed, the priority mixer 13 decides for each input port whether to pass on to a second pipeline stage 11 the requests RVi not satisfied by the first pipeline stage or any or all of the new requests RV2i received directly by the priority mixer. It is significant that the decision by the priority mixer 13 is made independently of the priority levels of the requests; as a result, the decision can instead be made based on whichever set of requests has the highest number of requests that could still be satisfied within the current connection vector CVi, taking into account which input and output ports of the switch are already used by satisfied connection requests.

In other words, prioritization and fairness of the priority selector come from presenting requests of only one priority level to the first pipeline stage 10 at any one time, where higher priority requests are presented proportionately more often than lower priority requests. The efficiency of the priority selector comes from mixing up priorities (by the priority mixer 13) in the second and subsequent pipeline stages, where priorities of requests are ignored and any currently unused output ports i.e. output ports not allocated a connection in the first pipeline stage 10, can be connected to any input port that has a request of any priority for that output port.

The claimed invention, in fact, includes a "priority mixer for determining a further set of said requests, the further set including requests of said first set which were not satisfied and requests included in said plurality of requests which were not part of said first set and which are of any of said priority levels, independently of said priority levels." Thus, the claimed invention recites that the first pipeline stage satisfies requests in dependence on priority, whereas as a result of operation of the priority mixer, subsequent pipeline stages satisfy requests irrespective of the priorities of the requests. This configuration enables the subsequent pipeline stages to satisfy requests so that efficiency of the switch is maximized.

To the contrary, Cloonan merely discloses a controller including a plurality of pipe controllers (24_0 to 24_3) connected in a ring. Each of these pipe controllers is identical and is the first stage encountered for some requests and the second or subsequent stage for other requests (dependent on the source and destination of the request). Requests for connecting

are injected into each of the pipe controllers (24_0 to 24_3) based on their destinations, and those requests are expected to circulate around all of the pipe controllers. Any requests not satisfied in an ATM cell time (switch cycle) result in the corresponding data packets being lost.

The Office Action asserted that the controller 24_1 of Figure 15 anticipates the claimed priority mixer of the present invention because Cloonan teaches to include requests R'_{EFGHi} and R''_{EFGHi} that are of different priorities in addition to those requests not previously satisfied. However, as explained above, the claimed priority mixer is operable to determine requests of all priority levels, independently of the priority of any particular request. In fact, the prioritization is achieved by the first pipeline stage.

Applicants submit that Cloonan fails to disclose, teach or suggest such a first pipeline stage for receiving a first set of requests (determined according to respective priority levels) and a priority mixer for determining a further set of requests including unsatisfied requests from the first set and requests of any of the priority levels, independently of the priority levels. Therefore, the claimed invention, as recited in independent claim 1 and its dependent claims 2-8 is patentable over Cloonan.

All rejections and objections have been addressed. It is respectfully submitted that the present application is now in condition for allowance, and a notice to that effect is earnestly solicited. Should there be any questions or concerns regarding this application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
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